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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/621,012
Filing Date: July 15, 2003
Appellant(s): RYAN ET AL.

Daniel Venglarik
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 07/27/07 appealing from the Office action mailed 2/28/06.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The amendment after final rejection filed on 08/10/06 has been entered.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,907,514	Mitsuishi	6-2005

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-6, 8-9,12-17, and 20-26 are rejected under 35 U.S.C. 102(e) as being anticipated by Mitsuishi, US 6907514. The rejections are maintained.

As per claims 1, 12, and 26, Mitsuishi teaches an integrated circuit comprising: a processor operable to issue memory access requests (e.g., fig. 1, microcomputer 1, CPU 2, col. 12, lines 55-60) each memory access request identifying an address in memory to which the request is directed (e.g., col. 18, lines 23-45; col. 14, lines 5-65); at least one on-chip resource falling within the address space addressable by the processor (e.g., col. 18, lines 23-45; col. 14, lines 5-65); an interface for directing packets off-chip and addressable within the address space of the processor (e.g., fig. 1, controller 12,); and a request directing unit for receiving said memory access requests and directing them in accordance with a selected one of first and second address maps (e.g., fig. 4, col. 18, lines 23-40), wherein said first address map has a first range of addresses allocated to said at least one on-chip resource and a second range of

addresses allocated to said interface (e.g., fig. 4, col. 18, lines 23-40), and in said second memory address map said first range of addresses are also allocated to the interface (e.g., fig. 4, col. 18, lines 23-40); and an off chip circuit connected to said interface and including at least one off chip memory resource (e.g., fig. 9, 105, 103, 101)

As per claim 20, Mitsuishi teaches a method of evaluating a prototype system comprising an integrated circuit including an on-chip processor (e.g., fig. 1, CPU 2) associated with at least one on-chip memory resource (e.g., fig. 1, RAM 6, ROM 5) and an off-chip circuit associated with at least one off-chip memory resource (e.g., fig. 9, RAM 101), the method comprising: executing a computer program on the on-chip processor, said program causing the generation of memory access requests (e.g., col. 5, lines 48-55), each memory access request including an address identifying an address in memory to which the request is directed (e.g., col. 18, lines 23-30); and in accordance with a selected mode of operation, selectively supplying said memory access requests to at least one of said first and second memory address maps (e.g., col. 18, lines 23-45), and directing the memory access requests selectively to said on-chip memory resource or said off-chip circuit in dependence on the selected one of said first and second address maps (e.g., fig 4, MSROM, MSRAM or EXTA col. 18, lines 23-50).

As per claims 2, 8, 13, 21, Mitsuishi teaches an integrated circuit according to claim 1, which comprises a mode setting pin for selectively setting a first mode in which said first address map is utilized and a second mode in which said second address map

is utilized (e.g., fig. 4, mode; col. 18, lines 23-40); wherein said mode is set by application of a logic value selected from one and zero on the mode setting pin (e.g., fig. 4, mode; col. 18, lines 23-40) .

As per claims 3, 4, 14, Mitsuishi teaches wherein said request directing unit comprises switching means responsive to a mode setting signal for selectively directing the memory access request to one of said first and second address maps (e.g., fig. 4, And gates and Mode); said switching means comprises a multiplexer (e.g., fig. 4, And gates and Mode).

As per claims 5, 15, Mitsuishi teaches wherein said at least one on-chip resource comprises a memory mapped peripheral (e.g., col. 18, lines 23-30).

As per claims 6, 16, Mitsuishi teaches wherein said at least one on-chip resource comprises a memory access device connectable to an off-chip memory resource (e.g., fig. 1, RAM 5).

As per claims 9, 17, Mitsuishi teaches wherein said interface comprises at least one chip-side port for transmitting memory access requests in parallel across a plurality of pins, and first and second circuit-side ports each with a reduced number of pins for communicating said packets off-chip (e.g., fig. 1, I/O ports).

As per claim 22, Mitsuishi teaches wherein said memory access requests are directed off-chip via an interface whose address space replaces the address space of the on-chip memory resource in the second memory address map (e.g., fig. 4, mode; col. 18, lines 23-40).

As per claims 23-25, Mitsuishi teaches wherein said memory access requests take the form of packets (e.g., col. 3, lines 30-35); wherein packets are chopped into chunks and transmitted in a plurality of cycles when being conveyed off-chip (e.g., col. 3, lines 30-35); wherein chunks received in a plurality of cycles from the off-chip circuit are reassembled into packets for transmission on-chip (e.g., col. 3, lines 30-35).

3. Claims 7, 10-11, and 18-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

(10) Response to Argument

Appellant's arguments filed 7/27/07 have been fully considered but they are not persuasive.

1. Appellant has not argued the rejections of claims 20-25; therefore, the Appellant has conceded that the examiner's rejection over claims 20-25 is proper.

2. Appellant argued with respect to independent claims 1,12, and 26 that the feature "the first range of addresses map to an on- chip resource in the first address map while that same first range of addresses map to the interface in the second address map; only the second range of address map to the interface in the first address map" is not found in the cited reference (Appeal brief filed 7/27/07, third paragraph, page 18).

In response to appellant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which appellant relies (i.e., while that same first range of addresses map to the interface in the second address map; **only** the second range of address map to the interface in the first address map) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

What the claims actually recite is "wherein said first address map has a first range of addresses allocated to said at least one on-chip resource and a second range of addresses allocated to said interface, and in said second memory address map said first range of addresses are also allocated to the interface". Nothing in this claim limitation precludes additional ranges of addresses being mapped to the interface in the first address map. In this case, Mitsuishi clearly teaches "wherein said first address map has a first range of addresses allocated to said at least one on-chip resource and a second range of addresses allocated to said interface (e.g., fig. 4, col. 18, lines 23-40),

and in said second memory address map said first range of addresses are also allocated to the interface (e.g., fig. 4, col. 18, lines 23-40)".

Moreover, even if one were to assume that appellants overly narrow interpretation of this claim interpretation is correct, Mitsuishi also teaches the first range of addresses map to an on- chip resource in the first address map (e.g., fig. 2, area 7, address range H' E00000-H'FFFFFF map to an on chip RAM 6; fig. 1, RAM 6 and col. 14, lines 8-10) while that same first range of addresses map to the interface in the second address map (e.g., fig. 2, area 7, addresses range H' E00000-H'FFFFFF maps to an I/O interface (ports, means, registers) via an interface 12 including external bus controller 121 and EXMDAC 4 or maps to an external device via I/O means; fig. 1, controller 12, IOP and col. 14, lines 15-30; col. 17, line 60 to col. 18, line 15); only the second range of address map to the interface in the first address map (e.g., fig. 2, only areas 2-5 addresses range H'400000-H'BFFFFF map to external device DRAM via interface 12 including external bus controller 121 and EXMDAC 4 and via I/O means; col. 14, lines 45-50; col. 16, lines 25-30; col. 12, lines 1-5).

3. Appellant further argued that Mitsuishi does not show two different address maps and Fig. 2 illustrates only a single address map.

The examiner disagrees with the Appellant's arguments because Mitsuishi, col. 2, lines 60-65, teaches "FIG. 2 is a diagram showing address maps" and col. 10, line 5, "FIG. 2 is a diagram showing address maps of the micro-computer."

Using the broadest reasonable interpretation, a map is a correspondence of elements in one set to elements in the same set or another set. Therefore, Mitsuishi teaches a first address map wherein, as shown in Fig. 2, area 7 (address range H' E00000-H'FFFFFF) maps to an on chip RAM 6. Mitsuishi further teaches a second address map wherein, as shown in Fig. 2, areas 2-5 (addresses range H'400000-H'BFFFFF) maps to an external device DRAM via interface 12 (which includes external bus controller 121) and via 1/0 means (col. 14, lines 45-50; col. 16, lines 25-30). Mitsuishi additionally teaches that the second map maps area 7 to the I/O means. Accordingly, Mitsuishi meets the language of the claims.

4. Appellant argued with respect to claims 1,12, and 26 that Mitsuishi does not disclose allocating one range of addresses to an interface in a first mode and allocating another range of addresses to that same interface in a second mode.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., in a first mode, in a second mode) are not recited in the rejected claim(s) 1,12, and 26. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

What the claims actually recited is "said first address map has a first range of addresses allocated to said at least one on-chip resource and a second range of addresses allocated to said interface and in said second memory address map said first

range of addresses are also allocated to the interface." Nothing in this claim limitation recites allocating one range of addresses to an interface in a first mode and allocating another range of addresses to that same interface in a second mode.

As discussed above in response to item 3, Mitsuishi clearly meets the actual claim limitations.

Also, according to, figs. 2, 4 and col. 18, lines 23-40, Mitsuishi shows selecting one of a first address map (address of an internal device, ROM5) and a second address map (address of an external space) wherein the first address map has a first range of addresses (Areas 0-1, address range H'000000-H'3FFFFF) allocated to said at least one on chip resource (ROM 5) and a second range of addresses (Areas 2-5) allocated to said interface (DRAM via EXTA to external controller interface 121 or via I/O means). See col. 14, lines 45-50; col. 16, lines 25-30; col. 12, lines 1-5. Further, the second memory address map maps said first range of addresses to said interface.

With respect to claims 2 and 13, in response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (allocating one range of addresses to an interface in a first mode and allocating another range of addresses to that same interface in a second mode.) are not recited in the rejected claims 2 and 13. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). What the claims actually recite is "a mode setting pin for selectively setting a first mode in which said first address map is utilized and a second mode in which said second

address map is utilized (e.g., fig. 4, mode; col. 18, lines 23-40). In this case, according to claims 2 and 13 the allocation was done initially, and after the initial allocation the first and second maps can be selected based on the mode. Nothing in this claim limitation recites which resource or interface is being used when selecting the first mode and the second mode. In this case, Mitsuishi clearly teaches "a mode setting pin for selectively setting a first mode in which said first address map is utilized and a second mode in which said second address map is utilized (e.g., fig. 4, mode; col. 18, lines 23-40)".

5. Appellant argued that with respect to claims 1,12, and 26, Mitsuishi does not teach that first and second address ranges are allocated to the I/O ports in different modes.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (first and second address ranges are allocated to the I/O ports in different modes) are not recited in the rejected claim(s) 1,12, and 26. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). What the claims actually recited is "said first address map has a first range of addresses allocated to said at least one on-chip resource and a second range of addresses allocated to said interface and in said second memory address map said first range of addresses are

also allocated to the interface." Nothing in this claim limitation recites first and second address ranges are allocated to the I/O ports in different modes.

6. Appellant argued that Mitsuishi does not teach a single address range that is mapped to an on chip resource in one mode and to an interface in a second mode. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (mapped to an on chip resource in one mode and to an interface in a second mode) are not recited in the rejected claim(s) 1,12, and 26. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). What the claims actually recited is "said first address map has a first range of addresses allocated to said at least one on-chip resource and a second range of addresses allocated to said interface and in said second memory address map said first range of addresses are also allocated to the interface." Nothing in this claim limitation recites a single address range that is mapped to an on chip resource in one mode and to an interface in a second mode.

7. Appellant argued with respect to claim 1, 12, and 26 that either of the two addresses ranges can be allocated first to ROM5 in one mode and then to input/output ports 21-26, 31-35 in a second mode.

The examiner agrees with Appellant's contention; however, there is nothing in claims 1, 12 or 26 that preclude both of the address ranges being mapped to both the

ROM5 and the I/O. Rather, the claims merely require that at least one of the address ranges be allocated to both.

8. Appellant argued with respect to claims 2 and 13 that Mode contributes to a device select signal, not an address map selection signal.

The examiner disagrees with the appellant's argument. According to fig. 4, and col. 18, lines 23-40, the combination of address IA23-IA0 and Mode, ROME pins for selecting an address (ROM 5 or RAM 6) which is a first address map (MSROM, MSRAM) and I/O means (MSIO) which is a second address map.

9. Appellant argued with respect to claims 3 and 14 that the cited reference does not teach Multiplexer 40 controls which address map (48,50) receives addresses for memory access requests and Mitsuishi discloses no switching circuitry for switching between first and second address maps in response to the MODE signal.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (Multiplexer 40 controlling which address map (48, 50) receives addresses for memory access request) are not recited in the rejected claims 3 and 14. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). What the claims actually recite is "wherein said request directing unit comprises switching means responsive to a mode setting signal for selectively directing the

memory access request to one of said first and second address map." Nothing in this claim limitation recites multiplexer for controlling which address map. In this case, Mitsuishi clearly teaches wherein said request directing unit comprises switching means responsive to a mode setting signal for selectively directing the memory access request to one of said first and second address maps (see fig. 4, And gates and Mode).

10. Appellant argued that the cited reference does not teaches the feature in claims 9 and 17 and Mitsuishi does not disclose that any of input/output ports 21-26 or 31-35 have sufficient pins for parallel transmission of memory access request packets on the chip (processor) side by have a reduced number of pins on the circuit (off chip) side.

In response to appellant's argument that the references fail to show certain features of appellant's invention, it is noted that the features upon which applicant relies (i.e., have sufficient pins for parallel transmission of memory access request packets on the chip (processor) side by have a reduced number of pins on the circuit (off chip) side) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). What the claims actually recite is " wherein said interface comprises at least one chip-side port for transmitting memory access requests in parallel across a plurality of pins, and first and second circuit-side ports each with a reduced number of pins for communicating said packets off-chip. Nothing in this claim limitation recite have sufficient pins for parallel

transmission of memory access request packets on the chip (processor) side by have a reduced number of pins on the circuit (off chip) side.

In this case, Mitsuishi teaches "wherein said interface comprises at least one chip-side port for transmitting memory access requests in parallel across a plurality of pins, and first and second circuit-side ports each with a reduced number of pins for communicating said packets off-chip (e.g., fig. 1, I/O ports)." Mitsuishi teaches I/O pins (ports) for transferring data col. 11, lines 10-15. There is no teaching in Mitsuishi that an additional pin is added for doing nothing.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Denise Tran

PPE 2185

November 12, 2007

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